"Faster, Better, Cheaper" Technologies
Used in the Attitude and information Management Subsystem for
NASA's Mars Pathfinder Mission

1)avid Ii. Woerner, 1)avid 11. 1 .chman
Jet Propulsion I .aboratory
California Institute of Technology
Pasadena, California

Abstract

The "Faster, Better, Cheaper" thrust at NASA /JPL has pushed new technologies into spacecraft designed for interplanetary missions. This is especially true for "Discovery" class missions such as Mars Pathfinder. Pathfinder is set to land a spacecraft and microrover on the surface of Mars for a "low cost" (relative to Viking costs of 3.2 billion in FY92 dollars). Pathfinder spacecraft must be for $150M (FY92 dollars). Mars Pathfinder is designed to meet this budget and prove out technologies for long-term investigation of Mars and future low cost landings and missions on Mars.

The Attitude and Information Management (AIM) subsystem design takes advantage of new parts, components, commercial equipment and software, and commercial and military standards to achieve a "1; aster, Better, Cheaper" mission. Some of the new interplanetary spaceflight technologies that AIM will fly are:

1. commercial 1)C-DC converters,
2. a hard VM Ebus backplane,
3. Field Programmable Gate Arrays (FPGAs),
4. Electricall y Erasable PROMs (EEPROMs),
.5. the VxWorks operating system,
6. Dynamic RAMs in 1 ermetically-sealed Memory Cards,
7. and a rad-hardened, 22MI 1'S, RISC CPU.

The insertion of these technologies has enabled the AIM subsystem to be cheaply built to support landing of Pathfinder on Mars.

Mars Pathfinder Mission Overview

A single Mars Pathfinder flight system will be sent to Mars between December 4, 1996 and January 3, 1997. See figure one. The flight system will be launched on a 1)elta II rocket and land on July 4, 1997. The flight system is spin-stabilized throughout cruise, spinning at 2 rpm. '1 'he medium-gain antenna (MC; A) is aligned with the spin axis which is pointed at Earth for communications.

The flight system remains pointed at Earth during cruise except for maneuvers. Maneuvers can be performed axially, i.e., along the spin axis, or laterally, i.e., orthogonal to the spin axis. During an axial maneuver, the flight system is turned to a burn attitude within ± 60 degrees of the sun-spacecraft line. The flight system remains earth pointed during lateral maneuvers and pulses the thrusters when they rotate into alignment with the maneuver direction.

The flight system reaches Mars after 7 months in cruise. The brief sequence of events between cruise and surface operations is called Entry, Descent, and Landing, or EDL. Approximately 30 minutes before atmospheric entry the flight system jettisons the cruise stage, see figure one; the cruise stage carries the propulsion system, attitude sensors, cruise stage electronics, and cruise solar array.

Entry is at 7.6 km/s (17,100 mph) and the atmospheric entry angle is -14.8 degrees. (-90 degrees would be straight towards the center of Mars.) Atmospheric drag decelerates the spacecraft to a peak of 25 g's. Peak deceleration is reached at approximately 32 km altitude. The spacecraft continues to slow until approximately 10 km altitude when a parachute is deployed (at Mach 1.8, or 900 mph). Deceleration from the entry velocity to Mach 1.8 takes 100 seconds.

The spacecraft jettisons an ablative heatshield used for entry in preparation for landing. At 1500 meters altitude, a radar altimeter begins measuring altitude. At 50 meters, retro-rockets are fired to slow the lander to < 20 m/s and airbags (as in a car) are inflated, fully surrounding the lander. The parachute and rockets are released and the lander freefalls to the surface at 20 meters altitude.

After the lander touches down, the airbags slowly deflate, and AIM deploys the lander petals; see figure 2, The landing will occur at approximately 4 am Mars local time with the sun and earth below the horizon.

When the Sun rises the lander will scan the horizon with its camera (a stereoscopic imager) searching for the sun. The direction to the sun and the direction of the local gravity vector in the lander coordinate frame provides all of the information needed to locate the direction to the Earth in the lander coordinate frame. Once Earth is located, the lander can turn a high-gain antenna to Earth and begin transmitting the EDL data and begin preparing for surface operations. Operations scenarios include taking panoramic images of the landing site, deploying the microrover, collecting science and engineering data from the rover, collecting temperature and pressure measurements of the atmosphere, and collecting data on the magnetic properties of the windblown Martian soil.

The nominal mission is slated to last 30 Martian days,

AIM Overview

The AIM subsystem is required to perform the following tasks:

- Acquire the sun following separation from the launch vehicle
- Acquire stars for celestial attitude reference
- Point the spacecraft spin axis for communications over a fixed medium gain antenna
- Control the spacecraft attitude and spin rate during cruise
- Receive, process, and manage command and data streams, including the execution of stored nominal and contingency command sequences and recording critical telemetry
- Perform trajectory correction maneuvers using reaction control thrusters
- Execute all events for the Entry, Descent and Landing (EDL) phase including processing accelerometer data to identify time of parachute deploy, radar altimeter data to identify time of impact, and to fire all EDL pyrotechnic devices. AIM also collects and stores all science data collected during EDL.
- Provide sufficient engineering data in the telemetry stream to support ground operations and interpretation of science and Rover data
- Provide fault protection for spacecraft and AIM functions
- Control and collect data from the Imaging and Atmospheric Science Instruments subsystems
- Perform HGA earth acquisition following landing using imaging data to locate the sun
- Provide High Gain Antenna tracking of the earth
- Manage the Lander to Rover communications link and collect and store uplink and downlink data
- Perform image data compression

The AIM subsystem is composed of two modules--the Lander Module and the Cruise Stage Module, see figure three. The

Lander Module houses the computer and all electronics and equipment required for landed operations. The Cruise Stage Module contains all AIM electronics and equipment mounted on the cruise stage of the flight system and is jettisoned prior to atmospheric entry.

The AIM computer is an IBM RAD6000-SC (Single Chip) processor operating a VMEbus and is called the Mars Pathfinder Flight Computer (MFC), see figure 3, Lander Module. The MFC also operates a UART (1< S-232) interface driving a 9600 baud modem for communications with the Rover. The MFC executes all spacecraft software and uses the VxWorks operating system.

Non-volatile memory is provided on the PROM (Programmable Read Only Memory) assembly. The PROM assembly uses Electrically Erasable PROM (EEPROM) to store flight software, sequences, and mission critical data, all of which can be updated in flight.

The Power and Pyro Switching Interface (PPSIF) board provides the relay drive signals to the power distribution relays, shunt regulator, and pym switching unit of the PPS subsystem.

The AIM, Lander, and Cruise Stage Power Converter Units (A/L/CPCU) draw power from the flight system's power bus and provide conditioned power for all AIM assemblies. The PCU designs rely on commercially available DC-DC converters.

The RSDL, (Reed-Solomon Downlink) assembly is the telemetry port from the AIM to the Telecommunications subsystem. It appends a synchronization pattern to the front of each telemetry data frame and a Reed-Solomon encoding pattern to the end of each data frame.

The "uplink" board is the Hardware Command Decoder (HCD) board. The HCD is the uplink data port between the AIM and the Telecommunications subsystem (TEL). The HCD handles error-detection-

and-correction (EDAC). The HCD assembly also controls the two 1553B buses.

Two Remote Engineering Units (REUs) collect temperature data, analog signals, digital data from various locations on the spacecraft, and provides synchronization between the bus and many of the peripherals on the spacecraft. One REU is mounted in the lander module. The REUs digitize temperature and analog data and provide this information on request via the modified 1553 bus. Commands from the MFC to "out-board" peripherals are routed via the REUs; all digital input and output signals pass through an interface unit [Lander Interface (LIF) or Cruise Stage Interface (CSIF)].

The LIF collects data from and sends commands to the Radar Altimeter subsystem, Atmospheric Structure Instrument/Meteorology (ASI/MET) experiment, High-Gain Antenna Drive Electronics (HGADE), and Accelerometer (ACCEL) assemblies.

The CSIF collects data from and sends commands to the Star Scanner Electronics, Digital Sun Sensor Electronics (DSE), and Propulsion Drive Electronics (PDE).

"Faster, Better, Cheaper" Technologies

Several technologies used in the design of the AIM are new to interplanetary spaceflight--their use is a direct result of the "faster, better, cheaper" thrust at NASA.

DC-DC Converters

Commercially-available DC-DC converters were procured from Modular Devices, Incorporated (MDI). The converters are inexpensive and space qualified. in addition, because the converters are compliant with MIL-S'I'I)-461, "Requirements for Control of Electromagnetic Interference Emissions and Susceptibility" the Pathfinder flight

system can build a simple power bus at a significant cost savings over a well-regulated bus.

AIM is designed with 17 converters configured so 6 portions of the subsystem can be turned-off and on as required. The AIM power load can be matched to the power available from the battery and solar array. (he or two large expensive converters would have made this impossible. Control over power utilization translates directly into more science data returned, and distributed power systems for low-cost spacecraft require converters such as the ones designed into the AIM subsystem.

MDI converters are hybrids, and consequently, are more reliable than converters built from discrete componei its.

Each converter contains an EMI filter to meet MIL-STD-461. The input range is from 16 to 50 VDX' (28 VDC nominal) while regulating output to better than $\pm 2\%$ into a full load. Efficiency is typically better than 70% into a full load. Output ripple is 50 mV peak-twpeak on AI M's 5V converter's. These converters also operate with input transients of 80 VDC per MIL-STD-704.

All converters are can withstand an indefinite short-circuit and are protected against overvoltage. A converter latches the output when an overcurrent condition is sensed. A converter will resume normal operation if the short clears.

in this mode, a converter oscillates between shu t down and operating until the short opens. Oscillation is at 100 Hz between 0 amps out and 130% of rating. Output in this mode is 40% of the maximum rating.

overvoltage is sensed on the primary side of a converter so a converter malfunction and an externally supplied overvoltage condition can be detected. If a malfunction is detected, an overvoltage shutdown is performed. If an overvoltage condition is externally supplied, the converter shuts off, and if the overvoltage condition clears, the converter will start up.

Each converter is a self-colltaind, hermetically scald, thick film DC-DC converter. All components (filter capacitors included) and power transformers are contained within a single package typically measuring 2.1" x 1.3" x 0.5" and weighing 50-125 grams.

VMEbus

IEEE standard 1034-1987 specifics the VMEbus. AIM uses VME as the primary computer bus. Selecting the standard has given Pathfinder many benefits:

- Development costs are lower
- Parts are easy to procure,
- Low-power parts can be used,
- The standard is well known,
- Engineers know the standard--learning curves are virtually non-existent,
- No time is spent designing a bus from scratch,
- VMEbus single-board computers are commercially-available,
- Bus analyzers are commercially - available,
- Chassis are commercially available,
- One-third of the back plane is undefined by the standard accommodate ing features required in the AIM design.

Using the VMEbus standard has allowed the AI M development to be broken into several parallel development and test efforts. Since specialized, hard to get equipment is not used, electronics and software designers can get development and test equipment inexpensively. Each designer can then create unencumbered by not having to wait to get into a single development environment. This allows each designer to prove his design will work with all other VME designs--there is no long serial build process for bringing up the AIM electronics and software.

Field-Programmable-Gate Arrays (FPGAs)

Field-Programmable-Gate Arrays (FPGAs) were chosen to implement a majority of AIM's logic. See figure 3 for an assembl - by-assembly accounting of the number of FPGAs used. AIM uses the commercial - available ACTEL 1280A. Each 1280A provides 8000 gates.

The 1280A operates al speeds required for the Mars Pathfinder Flight Computer. The flight lot operates at the processor's 20 MHz high-end with margin.

The ACTEL 1280A dramatically reduces the parts counts in the AIM design and cases the workload on the designers. Logic in the 1280As is a monolithic design that can easily be simulated. Repeated simulations on the gate array designs have produced virt ually error-free designs; designs with errors can be rapidly fixed and boards can be updated by replacing a single part.

Simulation results are good enough to build engineering model assemblies from CAI) files. Electronics designers typically require three levels of development al JPL: breadboard, engineering model, and flight units. The breadboard has been eliminated. Wire-wrapped assemblies are also not needed.

The ACT'10, 1280A has not been radiation hardened; however, radiation tests revealed the following results:

Single-Event Upsets (SEU)	2 upsets/part/year (assuming 1000 S-module latches per part)[*]
Single-Event Latchup (SEL)	0

[*] The 1280A uses two types of logic module. The S-module is the sequential module. The C-module is the combinatorial module. The S-module is an order-of-magnitude more sensitive to radiation than the C-module.

All numbers quoted are worst case. 1 Ieavy ions were used for the radiation tests; Pathfinder is flying in a solar minimum and expects to see only a Galactic-Cosmic Ray (GCR) background. Flight software and fault protection has been designed to recover from the SEUs predicted for the FPGAs. in addition, any state machine in an FPGA is shadowed by a redundant state machine. Any SEU to a state machine will induce a board-level reset. This prevents a state machine from entering an unexpected state and remaining there.

EEPROMs

AIM uses Electrically-Erasable PROMs (EEPROMs) as a PC uses a hard disk. Programs and data are stored in them so the spacecraft can boot upon reset, and critical science and engineering data can be stored in them. PROM boards can be added to the AIM in two Mbyte increments up to six Mbytes--the baseline (at the time this paper was completed) is to fly two Mbytes. The board is designed to support a VMEbus design that can carry 8 Mbytes.

The Mars Pathfinder Flight Computer (MFC) is designed to begin executing from PROM following a reset. PROM boot code loads the MFC DRAM. When loading is complete, control passes to flight Software) in RAM,

Each PROM board is built up from 80 SEEQ 1 EEPROM memories. Each memory device is 256K in a 32Kx8 configurate ion. The parts do not have internal error-ctetecticm and correction (EDAC). An FPGA is provided with each PROM board which appends a 7-bit code to every 32 bits written to the PROM board. Single-bit errors are corrected during a read cycle; double-bit errors are not corrected, just detected. Either error produces an interrupt, Flight software can query a register on the PROM board to find the address of a single or double-bit error. The EDAC process can also be disabled by flight software as required.

The EEPROMs have write limits of ~10,000 writes. The flight software and test programs are designed to ensure we never write more than 5,000 times to a each address. The EEPROMs are rated to retain data for 10 years; the nominal Pathfinder Mission is 8 months.

The SEEQ parts write and react data at a single voltage. This eliminates any need for multiple power supplies common for most other EEPROMs.

Each PROM board has write protection which is control] ed by setting the appropriate bits in each board's control register.

A PROM board can be read at a nominal VME transfer rate--10 Mbytes/sec for AIM, and a board has a write cycle of 10 ms. Both cycles are 32-bits wide (the 1 'ROM board is an A32 VME slave). An interrupt is generated at the end of each write cycle. Flight software uses the interrupt as a "wake-up" call; flight software can execute other tasks in the interim.

Mechanically, each PROM board is configured as a mother-daughter bead pair. Each board is populated with 40 memories and data from the daughter board is bussed to and from the mother board via an internal bus operated by an FPGA.

Radiation testing has shown the EEPROMs to be latchup immune. The EEPROMs do not exhibit SEU sensitivity when they arc inactive. The SEU rates during continuous reads is -0.15 upsets/par[/year and continuous writes result in 475 upsets/parl/year (~100 SEUs/board/day if writes were continuously made). In flight, since the AIM subsystem stores flight software and critical data in, flight software has been designed to ensure no data Sets corrupted during a write or a react. 1 Each PROM board draws 2 watts and has a mass of 1.0 kg.

The PROM was designed at JPL.

VxWorks

VxWorks has been ported to the Mars Pathfinder Flight Computer (MFC) by WindRiver Systems under contract from JPL. It provides developers with a well-established development environment. Most spacecraft computers come with small or undeveloped operating systems and toolsets. Previous programs have had to develop operating systems from the ground up or rely on alpha-tested versions typically requiring several modifications and requalifications for flight.

VxWorks does not require repeated requalification. Only the qualification of MFC specific portions of VxWorks is required. The software works as portal, providing an MFC development environment with all of the tools, faci lit its, and services common to workstation development environments.

The VxWorks development environment includes the VxWorks kernal (including a multitude of runtime facilities) as well as a set of development tools. The short list (only those used either in flight or during development for Mars Pathfinder) of VxWorks features includes :

- real-time, multi-tasking kernal with preemptive scheduling
- standardized I/O system using "LINIX-like" device mechanisms
- semaphores, message queues, signals, watchdog facility
- file system support
- drivers for network devices, pipes, and local (I{ AM) based file systems
- utility libraries for linked lists, ring buffers, memory partitions, and floating point functions
- performance evaluation tools (WindView, Stethoscope)
- source 1 evel debugger

The real-time kernal provides multitasking with preemptive priority scheduling, intertask synchronization and communication, interrupt handling support,

watchdog timers, and memory management. The multitasking kernal uses interrupt-driven, priority -based task scheduling, and has fast context switching and low interrupt latency. Any subroutine can be spawned as a separate task, with its own context and stack. Each task can be suspended, resumed, deleted, delayed, and moved in priority. VxWorks supplies message queues, pipes, and signals.

The I/O system includes device drivers for serial communication lines, disks, RAM disks, pipes, and devices on a network VxWorks includes a buffered I/O package that includes UNIX-compatible routines. Drivers to implement common device protocols and file systems are included.

The function of the Mars Pathfinder software requires that many of the VxWorks facilities used in development also be included in the flight configuration. This includes the kerns] facilities for semaphores and message queues, watchdogs, the I/O facilities including pipes and the MSDOS file system.

Pipes form the basis for intertask communication. Each task communicates by sending "messages" to other tasks within the software. Interrupt handlers do the same. Semaphores are used to protect (the few) shad resources. '1 he watchdog service is the basis for a custom timer facility that sends messages to tasks synchronous with the Earth time.

The AI M subsystem uses EEPROM to store all software, configuration information, critical recovery and safety data, and some science data. Most of this information is stored as files. The MSDOS file system driver is used along with a custom designed EEPROM driver.

Utility libraries are used to lower development time and memory utilization. The interrupt handling support library is used by the AI M subsystem for hardware interrupts and software traps so assembly-level routines do not have to be written. Watchdog timers are used by callers to schedule execution of their rout ines a

specified number of ticks in the future. The VxWorks memory allocation library supplies memory management tools for dynamically allocating, freeing, and reallocating blocks of memory from a memory pod; blocks of arbitrary size can be set. VxWorks also provides the entire set of libraries specified in ANSI X3.159-1989.

Software performance can be evaluated in several ways. An execution timer can be used to time any subroutine or group of subroutines. CPU utilization can be reported including time spent at the interrupt level and idle time.

The use of the commercial version of VxWorks also allowed the use of more advanced tools. 'J his include WindView for performance and task interaction analysis and Stethoscope for performance analysis. in addition, the VxWorks source level debugger vxgdb was used extensively.

Mars Pathfinder Flight Computer (MFC)

The MFC was designed and built for JPL by Loral FSC. The MFC uses two unique technologies: DRAMs in hermetically - sealed packages and a RAD-6000SC CPU.

The MFC has enough memory and CPU performance to free AI M programmers from having to manage memory and CPU thruput--a large labor and money sink on projects using limited memory and slow processors,

Dynamic RAMs and Hermetically-sealed Memory Cards

The MFC carries 128 Mbytes of Dynamic RAMs (DRAMs) for the execution of flight software where static RAMs (SRAMs) have been used in the past. The DRAMs are mounted on the Mars Pathfinder Flight Computer (MFC), see figure 3. Programs and data are retrieved from Electrically - erasable PROMs (EEPROMs) at the time the computer is booted. Once loaded, all programs execute out of the DRAMs.

The DRAMs are 16Mb Luna-C memories from IBM and operate at 3.3V. The memories have a 4Mb x 4 configuration.

Each DRAM provides Error-Detection and Correction (EDAC) capable of removing single-bit errors and reporting double-bit errors during a read. Pathfinder uses the EDAC to protect against Single-Event Upsets (SEUs). Extensive testing of the Luna-Cs at Brookhaven has shown the SEU rate to be 5 correctable SEUs per part per day (worst case) for the Pathfinder environment--Pathfinder is launching in a solar minimum and expects to only see a GCR background. EDAC will remove all SEUs.

Radiation testing has also shown:

- Luna-Cs do not latchup
- Luna-Cs will not have weak cells
  induced by the GCR background
- Luna-Cs will not have stuck cells
  induced by the GCR background

Each part is constructed with redundancy latches that are meet during packaging to remove "weak" wordlines and bit-lines. During production screening, if a cell m wordline is shown to not retain data for more than 256 milliseconds (ms)(the MFC uses a refresh time of 32 ms; the refresh time exceeds the data retention time by a factor of 8) then a redundant cell or wordline is swapped in by burning a fuse in the die. The upset rate of a redundancy latch rises after its fuse has been blown by approximately a factor of 30.

To minimize the impact of harming the mission, the Luna-C DRAMs have been screened for a minimum of latches with blown fuses. The flight lot has been selected so that no more than 6 wordline swaps occur during the mission in the worst case,

If the GCR radiation causes a redundancy latch to change state in-flight, a wordline with good program and data is swapped out for a wordline that has never been written to. The DRAM EDAC test will fail on the

next read from that wordline. Corrupted data is passed to the CPU and results in an interrupt. Flight software is designed to reboot and write into the swapped wordline. Execution of flight software proceeds normally following the reboot.

The DRAMs are arranged into 18 stacks of four. Viewed from the side, the stacks are composed of four planes. Each plane in the stacks can store 32 Mbytes contiguously. The stacks are hermetically sealed into an aluminum-silicon carbide metal matrix case. The case is called the } Hermetically - sealed Memory Card (HMC). HMCs are built by Loral Federal Systems.

Before flight, HMCs are qualified to the following requirements:

Thermal Cycle	-55 to +100 deg C for 2000 cycles or 5(J% of the test sets fail
High Temperature Storage	125 deg C for 1000 hours
Autoclave	2 atmospheres at 120 deg C for 500 hours
Temperature /Humidity/ Bias	85 deg C and 85% relative humidity at 3.6V bias for 1000 hours
Thermal Vacuum	25 cycles from -35 to +70 deg C
Random Vibe	20 to 2000 117, (56.0 g rms in normal, 15.7 g rms in plane)
Mechanical Shock (pyro)	60g/100Hz to 300g/200Hz, to 3000g/2000Hz to 2000g/10000Hz

RAD-6000SC CPU

The RAD-6000SC processor is a high-performance 32-bit, radiation-hardened IBM RS/6000 processor manufactured on a Loral FSC QML line. The processor is a RISC machine that is the basis for the PowerPC™ architecture. The RAD-6000SC runs commercially available software and RS/6000 workstations are used as development workstations for flight software.

The RAD-6000SC uses a fixed point, floating point, branch processor, memory management, and I/O sequencer units--this CPU allows for concurrent operation of fixed point instructions, floating-point instructions, and branch instructions. The CPU is variable speed with rates of 1.25, 2..5,5, 10, and 20 MHz.

The RAD-6000SC can address 4 Gigabytes of virtual memory and comes with 128 Mbytes of real memory. The AIM subsystem uses only 16 Mbytes of the address space for the VME bus.

The RAD-6000SC has a 72-bit memory interface to the HMCs--64 bits of data plus 8 bits of sillglc-error-correctioll/dollllJle-error detection code. (This EDAC code is in addition to the code in the 1 JRAMs described above.)

For testing the RAD-6000SC comes with a Common-On-board-Processor interface, or COP interface. The COP interface supports logic and array self-tmt, array initialization, and debugging via a tool called RISCWatch that can be used to download software and read registers in the CPU.

The RAD-6000SC has been radiation tested to show:

Total Dose	> 2×10^6 rads (Si)
Single Event Upset (SEU)	~ 1×10^{-10} Errors/bit-day @ LET >80 MEV/mg/cm^2
Latchup	none

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The MHC draws between 2.5 and 10.0 watts depending upon the processor speed. The MHC mass is 0.9 kg.
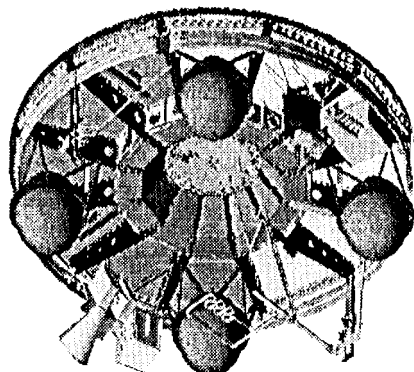
Conclusion

"Faster, Better, and Cheaper" technologies for interplanetary spaceflight arc readily available. The AIM subsystem is using many in its design that are rc'liable, flyable, and inexpensive. The technologies arc enabling new and exciting missions for NASA's future.

Cruise Stage

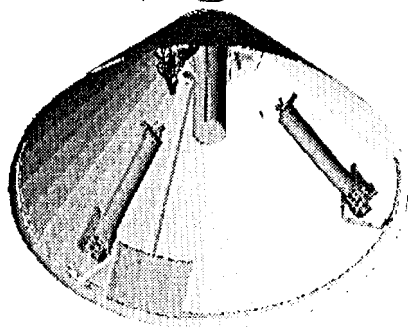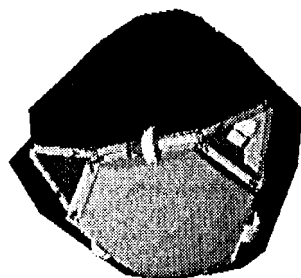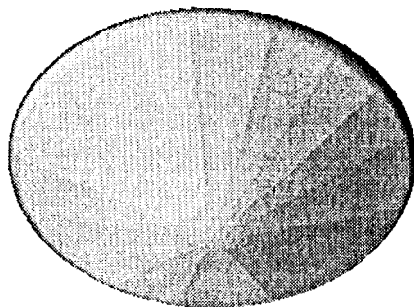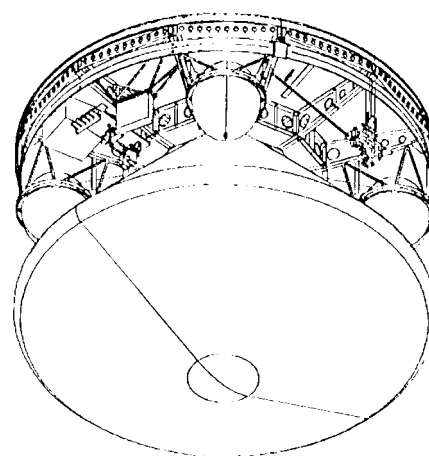Backshell

Lander

Heatshield

Exploded View

Cruise Configuration

Figure 1. Flight System

Figure 2

Figure 3

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